


WE CLAIM:

- 1  1. An integrated signal isolator having first  
2 and second ends, wherein the integrated signal isolator  
3 comprises:  
4 first and second isolator input terminals;  
5 first and second isolator output terminals;  
6 first and second power supply terminals;  
7 first, second, third, and fourth magnetoresistors,  
8 wherein the first and second magnetoresistors are coupled to  
9 the first isolator output terminal, wherein the second and  
10 third magnetoresistors are coupled to the first supply  
11 terminal, wherein the third and fourth magnetoresistors are  
12 coupled to the second isolator output terminal, and wherein  
13 the first and fourth magnetoresistors are coupled to the  
14 second supply terminal; and,  
15 an input strap having at least one turn coupled  
16 between the first and second isolator input terminals,  
17 wherein the input strap is disposed with respect to the  
18 first, second, third, and fourth magnetoresistors so that a  
19 magnetic field is generated over two of the magnetoresistors  
20 in one direction, so that a magnetic field is generated over  
21 the other two of the magnetoresistors in an opposite  
22 direction, and so that, when input current flows between the  
23 first and second isolator input terminals, a resistance of

24 the first magnetoresistor tracks a resistance of the third  
25 magnetoresistor, and a resistance of the second  
26 magnetoresistor tracks a resistance of the fourth  
27 magnetoresistor.

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1 2. The integrated signal isolator of claim 1  
2 wherein the at least one turn of the input strap is disposed  
3 with respect to the first, second, third, and fourth  
4 magnetoresistors so that, when input current flows between  
5 the first and second isolator input terminals, a first field  
6 is generated across the set/reset direction and two of the  
7 first, second, third, and fourth magnetoresistors and a  
8 second field is generated across the other two of the first,  
9 second, third, and fourth magnetoresistors and so that the  
10 first and second fields point in substantially opposite  
11 directions thereby producing an output across the first and  
12 second isolator output terminals commensurate with the input  
13 current.

1 3. The integrated signal isolator of claim 1  
2 wherein the input strap includes a plurality of turns.

1           4.    The integrated signal isolator of claim 3  
2    wherein each of the first, second, third, and fourth  
3    magnetoresistors comprises a serpentine structure having a  
4    plurality of elongated magnetoresistive portions coupled  
5    end-to-end, wherein the elongated portions of two of the  
6    magnetoresistors are position near and in parallel to a  
7    first elongated portion of each of the turns of the input  
8    strap, wherein the elongated portions of the other two  
9    magnetoresistors are position near and in parallel to a  
10   second elongated portion of each of the turns of the input  
11   strap, and wherein the first elongated portions of the turns  
12   of the input strap are parallel to the second elongated  
13   portions of the turns of the input strap.

1           5.    The integrated signal isolator of claim 3  
2    wherein each of the first, second, third, and fourth  
3    magnetoresistors comprises a serpentine structure having a  
4    plurality of elongated magnetoresistive portions coupled  
5    end-to-end, wherein the elongated portions of the first and  
6    second magnetoresistors are position near and in parallel to  
7    a first elongated portion of each of the turns of the input  
8    strap, wherein the elongated portions of the third and  
9    fourth magnetoresistors are position near and in parallel to  
10   a second elongated portion of each of the turns of the input  
11   strap, and wherein the first elongated portions of the turns

12 of the input strap are parallel to the second elongated  
13 portions of the turns of the input strap.

1 6. The integrated signal isolator of claim 1  
2 wherein the first, second, third, and fourth  
3 magnetoresistors are in a first layer, wherein the input  
4 strap is in a second layer, and wherein the first and second  
5 layers are separate layers.

1 7. The integrated signal isolator of claim 6  
2 further comprising a dielectric between the input strap and  
3 the first, second, third, and fourth magnetoresistors.

1 8. The integrated signal isolator of claim 7  
2 wherein the dielectric is a first dielectric, wherein the  
3 integrated signal isolator further comprises a second  
4 dielectric over the input strap, and wherein the first,  
5 second, third, and fourth magnetoresistors are formed over a  
6 substrate and under the first dielectric.

1 9. The integrated signal isolator of claim 1  
2 further comprising a set-reset coil having a plurality of  
3 clockwise turns and a plurality of counterclockwise turns,  
4 wherein each clockwise turn of the set-reset coil has a  
5 portion running across the first and fourth

6 magnetoresistors, wherein each counterclockwise turn of the  
7 set-reset coil has a portion running across the second and  
8 third magnetoresistors, and wherein the clockwise and  
9 counterclockwise turns are arranged so that current supplied  
10 to the set-reset coil flows through the portions of each of  
11 the clockwise and counterclockwise turns in the same  
12 direction.

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1 10. The integrated signal isolator of claim 1  
2 further comprising a set-reset coil having a plurality of  
3 turns disposed with respect to the first, second, third, and  
4 fourth magnetoresistors so that the set-reset coil generates  
5 a magnetic field across the first, second, third, and fourth  
6 magnetoresistors in the same direction.

1 11. An integrated signal isolator having first  
2 and second ends, wherein the integrated signal isolator  
3 comprises:

4 first, second, third, and fourth magnetoresistors,  
5 wherein the first and second magnetoresistors are coupled to  
6 a first isolator output terminal, wherein the second and  
7 third magnetoresistors are coupled to a first supply  
8 terminal, wherein the third and fourth magnetoresistors are  
9 coupled to a second isolator output terminal, and wherein

10 the first and fourth magnetoresistors are coupled to a  
11 second supply terminal; and,  
12 an input strap having at least one turn coupled  
13 between first and second isolator input terminals, wherein  
14 the least one turn has a first portion running alongside two  
15 of the magnetoresistors and a second portion running  
16 alongside the other two magnetoresistors, wherein the at  
17 least one turn is arranged so that current supplied to the  
18 input strap flows through the first portion in a first  
19 direction between the first and second ends and through the  
20 second portion in a second direction between the first and  
21 second ends, and wherein the first and second directions are  
22 substantially opposite to one another.

1 12. The integrated signal isolator of claim 11  
2 wherein the input strap includes a plurality of turns.

1 13. The integrated signal isolator of claim 11  
2 wherein the first, second, third, and fourth  
3 magnetoresistors are in a first layer, wherein the input  
4 strap is in a second layer, and wherein the first and second  
5 layers are separate layers.

1           14. The integrated signal isolator of claim 11  
2 further comprising a dielectric between the input strap and  
3 the first, second, third, and fourth magnetoresistors.

1           15. The integrated signal isolator of claim 14  
2 wherein the dielectric is a first dielectric, wherein the  
3 integrated signal isolator further comprises a second  
4 dielectric over the input strap, and wherein the first,  
5 second, third, and fourth magnetoresistors are formed over a  
6 substrate and under the input strap.

1           16. The integrated signal isolator of claim 11  
2 further comprising a set-reset coil having a plurality of  
3 clockwise turns and a plurality of counterclockwise turns,  
4 wherein each clockwise turn of the set-reset coil has a  
5 portion running across the first and fourth  
6 magnetoresistors, wherein each counterclockwise turn of the  
7 set-reset coil has a portion running across the second and  
8 third magnetoresistors, and wherein the clockwise and  
9 counterclockwise turns are arranged so that current supplied  
10 to the set-reset coil flows through the portions of each of  
11 the clockwise and counterclockwise turns in the same  
12 direction.

1           17. The integrated signal isolator of claim 11  
2 further comprising a set-reset coil having a plurality of  
3 turns disposed with respect to the first, second, third, and  
4 fourth magnetoresistors so that the set-reset coil generates  
5 a magnetic field across the first, second, third, and fourth  
6 magnetoresistors in the same direction.

1           18. A method of isolating first and second  
2 circuits comprising:

3           generating a first field across at least one  
4 magnetically responsive element, wherein the first field is  
5 generated in response to an isolator input signal from the  
6 first circuit;

7           generating a second field across at least another  
8 magnetically responsive element, wherein the second field is  
9 generated in response to the isolator input signal from the  
10 first circuit, and wherein the first and second fields are  
11 substantially opposite to one another in direction; and,

12           supplying an isolator output signal to the second  
13 circuit, wherein the isolator output signal is derived  
14 across the at least two magnetically responsive elements,  
15 and wherein the first and second fields are generated so  
16 that the isolator output signal is responsive to the  
17 isolator input signal that generates the first and second  
18 fields but not to an external field.



19. The method of claim 18 wherein the first field is generated across the first and second magnetically responsive elements and the second field is generated across third and fourth magnetically responsive elements, wherein the first and second magnetically responsive elements are coupled to a first isolator output terminal, wherein the second and third magnetically responsive elements are coupled to a first supply terminal, wherein the third and fourth magnetically responsive elements are coupled to a second isolator output terminal, and wherein the first and fourth magnetically responsive elements are coupled to a second supply terminal.

20. The method of claim 18 wherein the first field is generated across the first and third magnetically responsive resistors and the second field is generated across second and fourth magnetically responsive resistors, wherein the first and second magnetically responsive elements are coupled to a first isolator output terminal, wherein the second and third magnetically responsive elements are coupled to a first supply terminal, wherein the third and fourth magnetically responsive elements are coupled to a second isolator output terminal, and wherein

11 the first and fourth magnetically responsive elements are  
12 coupled to a second supply terminal.

1 21. The method of claim 18 wherein the first  
2 field is generated across the first and fourth magnetically  
3 responsive resistors and the second field is generated  
4 across second and third magnetically responsive resistors,  
5 wherein the first and second magnetically responsive  
6 elements are coupled to a first isolator output terminal,  
7 wherein the second and third magnetically responsive  
8 elements are coupled to a first supply terminal, wherein the  
9 third and fourth magnetically responsive elements are  
10 coupled to a second isolator output terminal, and wherein  
11 the first and fourth magnetically responsive elements are  
12 coupled to a second supply terminal.

1 22. The method of claim 18 further comprising  
2 setting the magnetic moments of the at least two  
3 magnetically responsive elements in the same direction.

1 23. The method of claim 22 wherein the moment  
2 direction is substantially perpendicular to the first and  
3 second fields.

1           24. The method of claim 23 wherein the setting of  
2 the magnetic moments is momentary.

1           25. The method of claim 24 wherein the setting of  
2 the magnetic moments comprises setting the magnetic moments  
3 prior to generating the first and second fields.

1           26. A method of making an integrated signal  
2 isolator having first and second ends comprising:  
3           forming first, second, third, and fourth  
4 magnetoresistors in a first layer of an integrated structure  
5 so that the first and second magnetoresistors are  
6 substantially aligned along a first axis, so that the third  
7 and fourth magnetoresistors are substantially aligned along  
8 a second axis, and so that the first axis is offset from and  
9 parallel to the second axis;

10           coupling the first and second magnetoresistors to  
11 a first isolator output terminal;

12           coupling the second and third magnetoresistors to  
13 a first supply terminal;

14           coupling the third and fourth magnetoresistors to  
15 a second isolator output terminal;

16           coupling the first and fourth magnetoresistors to  
17 a second supply terminal;

18 forming an input strap in a second layer of the  
19 integrated structure so that the input strap, when receiving  
20 an input, generates a field across two of the first, second,  
21 third, and fourth magnetoresistors and an opposing field  
22 across the other two of the first, second, third, and fourth  
23 magnetoresistors; and,

24 coupling the input strap between first and second  
25 isolator input terminals.

1 27. The method of claim 26 wherein the each of  
2 the first, second, third, and fourth magnetoresistors  
3 comprises a corresponding serpentine structure.

1 28. The method of claim 26 further comprising  
2 forming a dielectric between the input strap and the first,  
3 second, third, and fourth magnetoresistors.

1 29. The method of claim 26 further comprising  
2 forming a set-reset coil in a third layer of the integrated  
3 structure.

1 30. The method of claim 29 wherein the second  
2 layer is between the first and third layers.

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